DERWENT-ACC-NO: 2002-448353

DERWENT-WEEK: 200248

TITLE: Verification signal generator for semiconductor memory, e.g. RAM, has pattern reversal circuit which reverses verification signal output from test pattern generation device and outputs to memory device having different number of columns

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2002100200 A	April 5, 2002	N/A	011	G11C 029/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
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INT-CL (IPC): G01R031/28, G01R031/3183 , G06F012/16 , G11C029/00

ABSTRACTED-PUB-NO: JP2002100200A

BASIC-ABSTRACT:

NOVELTY - A test pattern generator (6) generates basic pattern which is applied to a memory device having different number of columns, for verifying each memory cell. A pattern reversal circuit (30) containing exclusive-OR gates (17,18), reverses the verification signal received from the test pattern generator and outputs the reversed verification signal to the memory device.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Semiconductor integrated circuit verification device;

(2) Verification signal generation method; and

(3) Semiconductor integrated circuit verification method.

USE - Used for verification of semiconductor memory e.g. RAM, DRAM, SRAM, etc.

ADVANTAGE - Enables simultaneous verification of memories within a short time using a checkered system, even if they have different number of columns.

DESCRIPTION OF DRAWING(S) - The figure shows the circuit diagram of semiconductor integrated circuit verification circuitry. (Drawing includes non-English language text).

Test pattern generator 6

Exclusive-OR gates 17,18

Pattern reversal circuit 30

CHOSEN-DRAWING: Dwg.1/11

TITLE-TERMS: VERIFICATION SIGNAL GENERATOR SEMICONDUCTOR **MEMORY** RAM PATTERN **REVERSE** CIRCUIT **REVERSE** VERIFICATION SIGNAL OUTPUT **TEST PATTERN** GENERATE DEVICE OUTPUT **MEMORY** DEVICE NUMBER COLUMN

DERWENT-CLASS: S01 T01 U14

EPI-CODES: S01-G01A1; T01-H01C; U14-D01;

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